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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/053,543 | 01/24/2002 | Masahiro Shimizu | 57454-329 | 3990 |

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McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

| EXAMINER |
|---|
| PERALTA, GINETTE |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/053,543 | SHIMIZU ET AL. | |
| | Examiner | Art Unit | |
| | Ginette Peralta | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will epply end will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *11-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/119,053* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Todorobaru et al. (U. S. Pat. 6,031,288) in view of Applicant's admitted prior art.

Regarding claim 11, Todorobaru et al . teaches in figs. 3-23 a method of manufacturing a semiconductor device that comprises the steps of:

a. forming a first and second gate electrodes (8A, 8B, 8C) of first and second transistors on a main surface of a semiconductor substrate 1 with a space between each other;

b. forming a nitride film 50 covering the first and second gate electrodes (8A, 8B, 8C);

c. forming source-drains (9,10,11) of the first and second gate electrodes (8A, 8B, 8C);

d. forming an interlayer insulating film 23 covering the nitride film 50;

e. forming in the interlayer insulating film 23 a first contact hole 24 reaching one of the source/drain of the first transistor;

f. providing a second contact hole (26,27,28,29) formed in the interlayer insulating film 23 and reaching one of the source/drain of the second transistor;

g. forming a bit line BL connected via the first contact hole 24 to one of the source/drain of the first transistor, and first and second interconnections extending into a second and a third contact holes.

Todorobaru et al. teaches all the limitations in the claim with the exception of forming a contact hole penetrating the interlayer insulating film and the nitride film reaching the second gate electrode.

Applicant's admitted prior art teaches in Fig. 37B and pages 1-4 of the applicant's specification a method of manufacturing a semiconductor device, that includes forming a contact hole penetrating the interlayer insulating film and an oxide cap layer reaching a second gate electrode, wherein an interconnection is formed in the contact hole for the well known intended purpose of connecting the gate electrode to other areas of the circuit.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a contact hole and an interconnection reaching the gate electrode directly in order to connect the gate electrode to other parts of the circuit as it is a well known and common practice in the art, and as taught by the conventional method of the Applicant's admitted prior art.

Regarding claim 12, Todorobaru et al. teaches in figs. 23, that the source/drain of the second transistor having a highly doped region, wherein the step of forming the

source/drain of the second transistor includes the step of forming a first metal silicide 35A at a surface of the heavily doped region; and the step of forming the bit line BL includes the steps of forming a plug electrode 25 in the first contact hole; forming a second metal silicide 35B at a surface of the plug electrode 25, and forming the bit line on the second metal silicide 35B.

3. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Todorobaru et al. in view of Kim et al. (U. S. Pat. 6,087,215).

Todorobaru et al . teaches in figs. 3-12 a method of manufacturing a semiconductor device that comprises the steps of:

h. forming a first and second gate electrodes (8A, 8B, 8C) of first and second transistors on a main surface of a semiconductor substrate 1 with a space between each other;

i. forming a nitride film 50 covering the first and second gate electrodes (8A, 8B, 8C);

j. forming impurity regions (9,10,11) at opposite sides of the first and second gate electrodes (8A, 8B, 8C);

k. forming an interlayer insulating film 52 covering the first and second electrodes (8A, 8B, 8C);

l. forming in the interlayer insulating film 52 a first contact hole 55 reaching one of impurity regions of the first transistor;

m. forming a storage node electrically connected to the impurity region through the contact hole.

Todorobaru et al. teaches all the limitations of the claim with the exception of introducing impurity into the semiconductor substrate through the contact hole to form a second impurity region overlapping with the first impurity region.

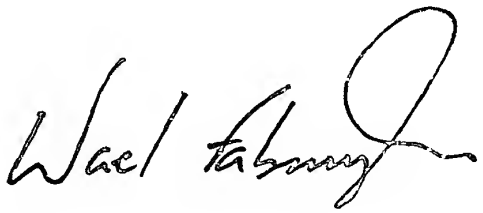
Kim et al. teaches in figs. 3a-3d a method of manufacturing a semiconductor device that includes forming first and second gate electrodes 25, forming impurity regions (26A, 26B), forming an insulating layer 27 over the gate electrodes, forming a contact hole 29, and introducing impurity into the semiconductor substrate through the contact hole to form second impurity regions 30 overlapping with the first impurity regions, and forming a storage node electrode 28 electrically connected to the second impurity region through the contact hole (col. 5, ll. 32-35), wherein the implant through the contact hole is performed for the disclosed intended purpose of reducing the junction leakage of a junction interface by increasing the depletion depth of the impurity region and reducing the electrical field of the impurity region.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implant impurities through the contact hole, as Kim et al. teaches that this step would result in reducing the junction leakage of a junction interface by increasing the depletion depth of the impurity region and reducing the electrical field of the impurity region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (703)305-7722. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703)308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.



SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800

GP
November 15, 2002